# TEST PLAN for “Generate blocks” in IEEE format

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# IEEE TEST PLAN

## TEST PLAN IDENTIFIER

* This test plan is for testing generate blocks which are new feature in VHDL. for generate block can be used when the designer needs to replicate logic in VHDL. if generate block can be used when the designer needs to turn on/off logic in VHDL

## REFERENCES

* + 1. IEEE Standard VHDL Language Reference Manual, September 26, 2008
    2. Cadence assertion writing guide, March 2015
    3. Property Specification Language Reference Manual v1.1, June 9, 2004
    4. Peter J. Ashenden, VHDL 2008: Just the New Stuff (Systems on Silicon) 1st Edition, November 26, 2007

1. **INTRODUCTION**

* This test plan is for testing a new release of the simulator which is planning to support the VHDL “generate blocks” in VHDL language which was not supported by our previous release. that generate block feature has three types: “For generate”, “If generate” (modified feature) and “case generate” (new feature).

## TEST ITEMS (FUNCTIONS)

1. simple generate blocks (for, if and case).
2. Generate block with user errors
   * For generate using floating index.
   * For generate using dynamic index.
   * For generate using negative index.
3. Generate block using overlapped index.
4. Generate block using generic.
5. Multiple generate blocks
   * For then for.
   * If then if.
6. Nested generate blocks from different type
   * For nested if.
7. Generate blocks using complex condition.
8. Nested generate blocks from the same type
   * For nested for.
   * If nested if.
9. Sequential generate block and another combinational one
10. Generate block which has sequential and combinational blocks
11. **FEATURES TO BE TESTED**

* “For”, “if” and “case” generate Blocks using VHDL with PSL assertion.

## APPROACH (STRATEGY)

* My approach in testing generate blocks using VHDL with Property Specification Language (PSL) assertion is to test the common different scenarios of using generate blocks in digital IC design and verification and to test the common mistakes that user may do and compare my expectation about this mistake by the debugging of the tool.

## ITEM PASS/FAIL CRITERIA

* I expected the output of each single case based on the generate block functions and syntax and the purpose that designer use it for. Then, I compared this expectation by the debugging of the tool.

## TEST DELIVERABLES

* Test Plan in IEEE test plan format
* VHDL codes of 10 different test cases.
* Presentation Slides.